A High-Speed, Low-Power Analog-to-Digital Converter in Fully Depleted Silicon-on-Insulator Technology

by

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Abstract

This thesis demonstrates a one-volt, high-speed, ultra-low-power, six-bit flash analog-to-digital converter fabricated in a fully depleted silicon-on-insulator CMOS technology.

Silicon-on-insulator CMOS technology provides a number of benefits for low-power low-voltage analog design. The full dielectric isolation of the silicon island, where the transistors are built, allows higher layout packing density and reduces parasitic junction capacitances. Fully depleted silicon-on-insulator (SOI) exhibits improved subthreshold slope, which allows for lower transistor threshold voltages. Significant savings in power consumption can be obtained by leveraging these advantages. However, the floating-body effect can create significant problems in analog circuits, leading to potential circuit malfunction.

A single-ended auto-zeroed comparator topology is optimized to leverage the advantages of fully depleted SOI technology and avoid the floating-body effect. Using this comparator topology and other circuit techniques that operate with a one-volt supply, a six-bit 500-MS/s flash A/D converter is designed with the lowest power-consumption figure of merit in its class. Consuming only 32 mA from a one-volt supply, the quantization energy figure of merit for this design is calculated to be $E_Q = 2$ pJ.

Test chips were fabricated in MIT Lincoln Laboratory's 0.25-μm fully depleted SOI CMOS process. Testing of this design demonstrates the potential of SOI technology for the production of high-speed, low-power analog-to-digital converters.

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